THE PROXIMITY OF MICROVIAS TO PTHs AND ITS IMPACT ON THE RELIABILITY

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Abstract

High Density Interconnect (HDI) technology is fast becoming the enabling technology for the next generation of small portable electronic communication devices. These methods employ many different dielectrics and via fabrication technologies. In this research, the effect of the proximity of microvias to Plated Through Holes (PTHs) and its effect on the reliability of the microvias was extensively evaluated. The reliability of microvia interconnect structures was evaluated using Liquid-To-Liquid Thermal Shock (LLTS) testing (-55^oC to +125^oC). Comprehensive failure analysis was performed on microvias fabricated using different via fabrication technologies. Test vehicles that were manufactured by multiple vendors were used in this study. The test vehicles incorporated microvias that were fabricated using different laser ablation and photoimaging technologies. Laser technologies, such as YAG laser drilling and YAG-CO_2 laser drilling, in non-glass reinforced and glass reinforced dielectric materials were evaluated. The resistance of the via chain was measured at various stages of LLTS testing. Samples that failed were subjected to non-destructive and destructive analysis in order to fully understand the failure mechanism. The effect of the plating thickness, via fabrication technology, dielectric material, and the effect of the proximity of microvias to the PTHs on the fatigue life was studied. It was found that the location of microvias vis-à-vis PTHs did have an effect on the reliability of microvias.

Introduction

The electronic packaging industry is moving towards developing advance packaging technology such as Chip Scale Packages (CSPs) and Direct Chip Attach (DCA). These packages enable more functions and information to be utilized in a smaller area. To accommodate high density packages, Printed Circuit Board (PCB) fabricators have been developing higher density circuit fabrication methods. Increased product functionality coupled with size reduction places extreme demands on the circuit designer to increase silicon integration and reduce PCB size. The trend towards portable electronics makes volume and weight prime factors. Above considerations forces PCB designers to design circuit boards with reduction in Radio Frequency Interference (RFI), Electromagnetic Interference (EMI), and crosstalk. Clock rates have increased to the GHz range. The PCB industry's first approach to increasing density was to add more layers using conventional through hole technology for the electrical inter layer connection. When the required density of fine line circuitry went below 7 mils, sequential lamination, and blind and buried via technologies were introduced [Arledge, 1998].

High Density Interconnect (HDI) technology is an enabling technology for the next generation of small portable electronic communication devices. HDI technology is based on various types of build up methods for the manufacture of multilayer boards. These methods employ many different approaches: a photoimageable dielectric, a laser ablated dielectric, or a resin coated copper foil with laser, photo or plasma etched via fabrication. In the microvia reliability program at Universal Instruments Corporation

(UIC), microvias were fabricated by laser ablation and photoimaging technologies supplied by multiple vendors for evaluation. Table 1 shows the microvia fabrication technology used in the test samples supplied by four different vendors and the summary of the failure modes observed for the respective technology. The effect of the via size and the via pad size on the reliability of the microvias were studied and reported in [Joshi, 2000]. The proximity of microvias to Plated Through Holes (PTHs) was suspected to have a detrimental effect on the reliability of microvias. The presence of fibers in the via area could lead to the migration of plating along the fibers which in extreme cases, could lead to shorts to an adjacent structure. Additionally, local CTE mismatch between the matrix fiber and copper PTH structure could lead to cracks in the resin or the plating in the microvia.

To evaluate the effect of the proximity of microvias to PTHs, a via proximity test structure was designed. Figure 1 shows the schematic and cross sectional view of the proximity of microvias to PTHs. These vias and PTHs are daisy chained separately to allow the continuity testing. Figure 1a shows the proximity effect test structure used for the evaluation. On a single test site, there are 3 PTH chains containing 18 PTHs per chain per PTH diameter. Five boards from each Vendor were subjected to LLTS testing. Figure 1b shows the schematic of the lay out of the PTH and microvias on the test vehicle. The PTH sizes tested were 20, 35, and 50 mils. The via size was held constant at 5 mils. The distance of the vias from the PTHs is varied from 5 mils to 40 mils in the increment of 5 mils. Effective center to center distance of vias from PTHs varies from 45 mils to 80 mils (for 50 mil PTH), from 36 mils to 71mils (for 35 mil PTH), and from 27 mils to 62 mils (for 20 mil PTH) in the increment of 5 mils. Table 1a shows the effective center to center distance of the via from the PTH.

Technology Used to Fabricate Vias

Representative microvia samples obtained from four vendors were cross sectioned. This was done to determine the quality of the microvias 'as received' and to study the shape of the microvias and the test structure before they were subjected to reliability experiments. The preliminary analysis that was conducted helped in understanding different via parameters including the via wall inclination angle, the top and bottom diameters, and the metallization thickness. This proved useful in understanding the capability of the technology in terms of plating quality and non-uniformity in the shapes of the different via sizes. Figure 2 shows the time zero cross sections of the microvias fabricated by different vendors.

Figure 2a shows a cross section of a YAG drilled microvia fabricated by Vendor D. Vendor D used only the YAG laser to fabricate vias. The build-up dielectric layer in the boards from Vendor D was non-reinforced (no glass fibers in the epoxy dielectric). The effect of the dielectric material used and the via formation technology on the failure mechanism is summarized in the Table 1.

Vendor L provided photodefined microvias for reliability evaluation. The boards from Vendor L were based on IBM's "Surface Laminar Circuit" (SLC®), sequentially laminating photoimageable dry film dielectric layers over a multilayer FR-4 sub-composite. Figure 2b shows a cross section of a microvia from Vendor L. It is observed in this cross section that the via wall angles are rather straight. The straight via wall is characteristic of the photo process.

The microvias from Vendor M were formed with a two-step laser process. The microvias were formed on the top copper layer on glass reinforced FR-4 dielectric, by using the combination of a YAG-CO_2 laser. YAG-CO_2 laser process is explained in [Sudhakar & Schreiner, 1998]. Vendor H supplied microvias fabricated by both YAG only and YAG-CO_2 laser. Microvias from Vendor H were drilled on the top copper layer using a YAG laser and dielectric was drilled using YAG laser and YAG-CO_2 laser in case of YAG only and YAG-CO_2 laser drilled vias respectively. The dielectric layer in the board is glass reinforced FR-4. The top copper layer as well as the inner dielectric layer was ablated using a YAG laser. Figure 2c and 2d show the cross section of a via fabricated by Vendor H. It can be observed from the cross section that the via walls have a positive slope that helps in uniform plating of YAG and CO_2 laser drilled vias. However, the shape is different as compared to drilled microvias that were drilled using a YAG laser.

Via Proximity Testing Methodology

Via proximity testing consisted of incoming inspection (initial electrical testing and visual inspection) and cross sectioning before and after thermal shock testing of the via chains. An incoming inspection of boards was performed to assess the overall integrity of the interconnection. During the incoming inspection of the testing samples, undrilled PTHs were observed in few samples from Vendor D. This was due to a first pass CAD error that was corrected and samples were provided for evaluation.

Figure 3a shows the cross section of a time zero via failure that had a break in the hole wall by Vendor D. This could be due to the entrapment of air bubbles during plating or the improper cleaning of plating resist residue. Figure 3b shows the cross section of an improperly plated via that resulted in a time zero failure in a board from Vendor D.

LLTS testing was used to assess the effect of the via proximity to PTHs on the reliability of the vias. This testing subjected the microvias on the test vehicle to extreme environmental conditions. Ideally, accelerated stress testing (LLTS) induces failure modes similar to the ones expected in the field use of that product, but within an abbreviated time scale. Each LLTS cycle consisted of a 5 minute dwell at each temperature extreme (-55^oC and +125^oC) with a transition time of 10 seconds.

The coupons containing the test sites were separated from the test vehicle before they were sent for LLTS testing. Incoming inspection was carried out on samples supplied by each vendor. This included comprehensive electrical testing performed to check the continuity of the via chains before they were subjected to LLTS testing. It was reported in [Joshi, 1999] that there were no failures until 500 LLTS cycles for vias of any size. The boards were subjected to LLTS cycling and removed from the chamber for electrical continuity testing. After 700 LLTS cycles, resistance measurements were carried out at intervals of 100 LLTS cycles. The samples were tested for 2000 LLTS cycles. A 20% increase from the initial via chain resistance was considered the failure criterion. This criterion was chosen due to the relatively low value of the resistance measurement. It should be noted that the pads used for via chain resistance measurements were highly oxidized when they are subjected to LLTS testing. These pads were cleaned with a copper cleaning solution (Kester copper Nu) prior to the resistance measurements.

Via Reliability Evaluation and Failure Analysis

This section of the report presents the via reliability evaluation and the failure analysis. Table 2 shows the number of failed vias at different distances from a PTH for Vendor M. The first failure was reported after 1100 LLTS cycles. Figure 4 shows the 3-dimensional plot for the PTH diameter (X-variable), vias distance from PTH (Y-variable), and number of failed vias (Z–variable) for Vendor M. It can be observed that the failure frequency of the vias at a distance of 40 mils from a PTH was found to be the greatest.

To understand the failure mechanisms, cross sections of the failed samples are presented in the following sections. Figure 5 shows the cross section of a failed microvias after different stages of LLTS cycles. Figure 5a shows the cross section of a failed microvia after 1100 LLTS cycles. This via was at a distance of 40 mils from a 20 mil PTH. It should be recalled that Vendor M used a YAG and a CO_2 laser to fabricate microvias. The CO_2 laser possesses high energy that debonds the glass fibers from the glass reinforced composite. The presence of fibers debonded in the via area has lead to the migration of plating along the fibers. The via structure at a distance of 5 mils (center to center distance of 27 mils from 20 mils PTH) from a PTH was examined to check for possible shorts to the PTH due to migration of plating along the debonded glass fibers. Although bias testing has not been performed, continuity testing of the unbiased samples showed no cases of migration or bridging.

To determine the failure mode after 2000 LLTS cycles, failed samples were cross sectioned and analyzed. Figure 5b shows the cross section of a via at a distance of 40 mils from a 50 mil PTH that failed after 2000 LLTS cycles. A crack can be seen through the via that caused the high resistance value. It is important to note that vias at a distance of 40 mils failed earliest. In addition, cracks can be seen in the cross section. As the testing progresses, these cracks propagate and lead to failures as shown in

Figure 5c. This figure shows the cross section of a via at a distance of 40 mils from a 50 mil PTH. A void in the plating can be seen in the cross section. In addition, cracks propagating from the periphery can be seen in the cross section.

Table 3 shows the number of failed vias at different distances from a PTH (Vendor L). It can be seen that the failure frequency of vias at a distance of 40 mils from a 50 mil PTH is higher than vias at a distance of 5 mils from PTH. Similar trends were observed in the vias near 20 mil PTHs. Figure 6 shows the 3-dimensional failure frequency plot for Vendor L. It shows that the failures were found at a distance of 40 mils from the PTH. In addition, several fails were found on samples at a location of 5 mils from the PTH. However, the failures at a distance of 40 mils from the PTH were more than the failures at a distance of 5 mils.

Figure 7 shows cross sections of a microvias from Vendor L after different stages of LLTS testing. Figure 7a shows a failure in a via at 40 mils from a PTH. The cause of failure was found to be a crack at the via-pad interface. Microetching of the cross sectioned sample was carried out to make the crack more visible. It was observed that the crack was initiated at the via-pad interface. Due to a sharp corner at the via-pad interface, it becomes a high stress concentration region and is susceptible to crack initiation. It can be seen that via wall angles are straight, which is characteristic of a photo defined via. It can be observed from Figure 7a that the plating thickness at the bottom of the via is slightly less than the plating thickness at the top. This could be due to the straight via walls. Negative slope can be observed from the cross section after the plating. This might result in a break at the via-pad interface in an extreme case [Joshi, 1999]. A similar failure was observed in the via at a distance of 5 mils from 50 mil PTH after 1100 LLTS cycles. Figure 7b shows the cross section of a functional via at a distance of 5 mils from a 35 mil PTH after 2000 LLTS cycles. Uniform plating thickness can be seen from the cross section.

Table 4 shows the number of failed vias in samples provided by Vendor D. It can be observed from the table that only 5 failures were reported. The samples were tested for 2000 LLTS cycles. The failed via was cross sectioned to determine the failure mode. Microetching of the cross sectioned sample was carried out to make the crack more visible as shown in the Figure 8. Again, it was observed that the crack was initiated at the via-pad interface.

It was observed that the vias at a distance of 40 mils from PTHs showed greater number of failures as compared to other vias. It should be remembered here that via size was held constant at 5 mils. It was observed that a crack at via and pad interface was a dominant failure mode. Figure 9 describes the mechanism behind higher frequency of failures observed in vias at the distance of 40 mils from PTH. It is proposed that the mechanical interlocking and Z-axis CTE of the copper PTH prevent the high CTE of the epoxy/glass layers from expanding. This in turn causes a local 'Z' axis constraint on the outer dielectric layers around the PTH. This reduces the occurrence of the main failure mode for microvia technology that is separation of via from the stop pad in case of vias at the distance of 5 mils from the PTH. Figure 10 shows the cross section of a 5 mil failed via near a 35 mil PTH after 1500 LLTS cycles. It can be clearly seen from the cross section that the via did not register on the stop pad and just managed to establish contact with the stop pad. A crack can be seen in the region circled in the photograph (Figure 10). It can also be seen that the YAG laser drilled down into the underlying dielectric. Additionally, the laser missed the stop pad and drilled down into the underlying dielectric layer that resulted in poor plating thickness at the bottom of the via. An inward curve can be seen from the photograph of the cross section that eventually resulted in a failure. It is interesting to see debonded glass fibers near the cracks.

Vendor H supplied samples that used both YAG and a YAG-CO_2 laser to fabricate vias in glass reinforced dielectric. No failures were observed in the samples from Vendor H until 2000 cycles of LLTS testing.

Conclusion

- The maximum failures were found in vias at a distance of 40 mils (60 mils center to center distance from 20 mils PTH) from the PTH. In addition, few failures were found in the vias at the distance of 5 mils from the PTH.

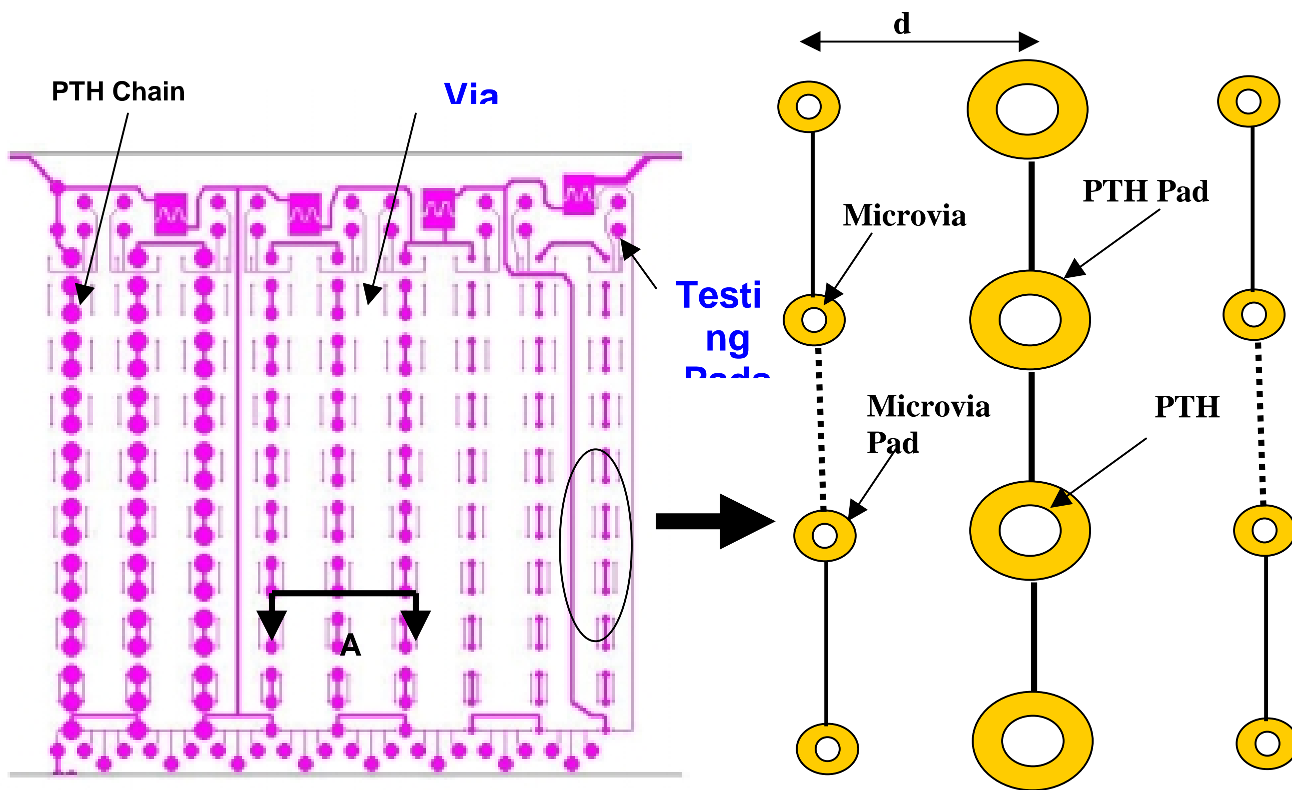
- The uncleaned epoxy and glass fibers in the via hole are a major cause of via failure. The time taken by a CO_2 laser to ablate dielectric is less than that required by a YAG laser. Thus, the CO_2 laser process might be more beneficial from a manufacturing standpoint.
- Misregistered vias (those that just manage to establish contact with the stop pad) affect reliability and result in early failure. This was observed for only YAG laser drilled vias from Vendor D. Hence, the YAG laser parameters used by Vendor D need to be optimized.
- Photodefined vias have straight via walls. This can cause problems during plating if the inward curve of the plated via walls results in a reduction of the plating thickness at the via bottom. The via-pad interface is one region of high stress concentration. The cumulative effect of a high stress concentration and poor plating could make this region susceptible to crack initiation. It was observed that cracks initiated at the via-pad interface and propagated resulting in a failure in most cases.
- Improper cleaning of the glass fibers in the glass reinforced dielectric was found to be a major cause of failures. Improper cleaning of the glass fibers in YAG+CO_2 laser drilled vias was found to be the dominant failure mechanism. In addition, a crack through the via plating was found to be the reason for the failure of the YAG+CO_2 laser drilled vias.
- Vias drilled in glass reinforced dielectric and non reinforced dielectric lasted for approximately the same time. However, the failure mechanisms were different in vias drilled in the glass reinforced and non-reinforced dielectric. Table 1 summarizes the via fabrication method, dielectric material used and the failure mechanisms observed.

References

1. Arledge, K., & Swirbel, T., “Microvias in Printed Circuit Design”, IPC Printed Circuits Expo, April 1998, pp. S08-1 – s08-8.

2. Joshi, J. “Reliability Evaluation and Proximity Analysis of High Density Microvia Structures”, Masters Thesis, State University of New York at Binghamton, Binghamton, New York, August 2000.

3. Sudhakar, R. & Schreiner, A., “UV Laser Drilling of Multilayer Blind Vias”, IPC Printed Circuits Expo, Long Beach, California, April 1998, pp. s17-1 – s17-8.



a. Top Down View of the Proximity Test

b. Layout of the PTHs and

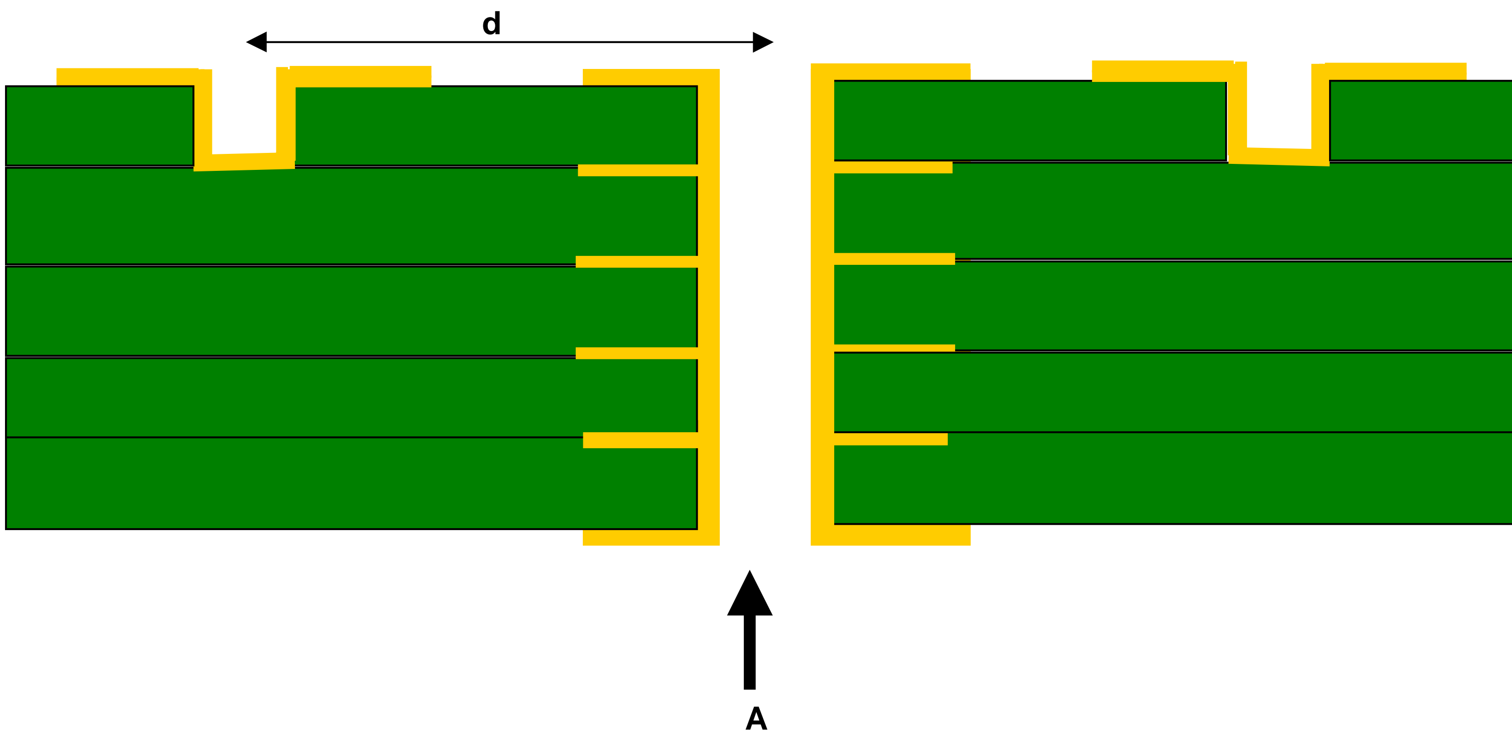
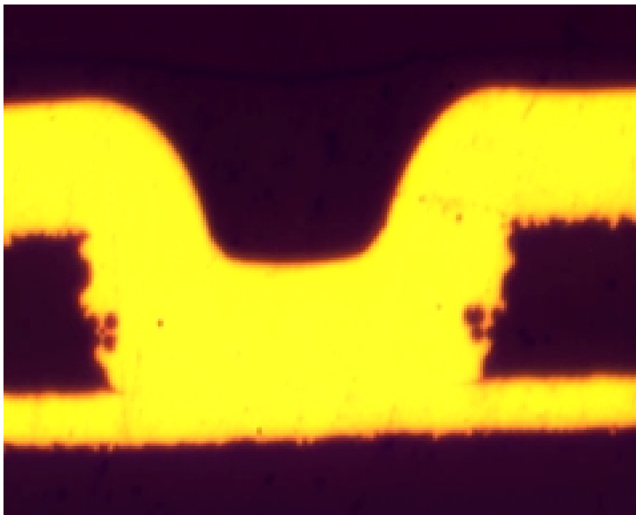


Figure 1. Schematic and Cross Sectional View Showing the Proximity of Microvias to PTHs

a. Cross Section of a YAG Laser Drilled Microvia from Vendor 1

b. Cross Section of a Photo Processed Via from Vendor 4



c. YAG and CO_2 Laser Drilled (Vendor 3)

d. YAG Laser Drilled (Vendor 2)

Figure 2. Time Zero Cross-Sections of Microvias Manufactured by Different Vendors

a. Cross Section of a Via with a Break in the Hole Wall (Time Zero Cross Section)

b. Cross Section of an Improperly Plated YAG Laser Drilled Via from Vendor 2 (Time Zero Cross Section)

Figure 3. Time Zero Electrical Failures due to Improperly Manufactured Microvias from Vendor 2

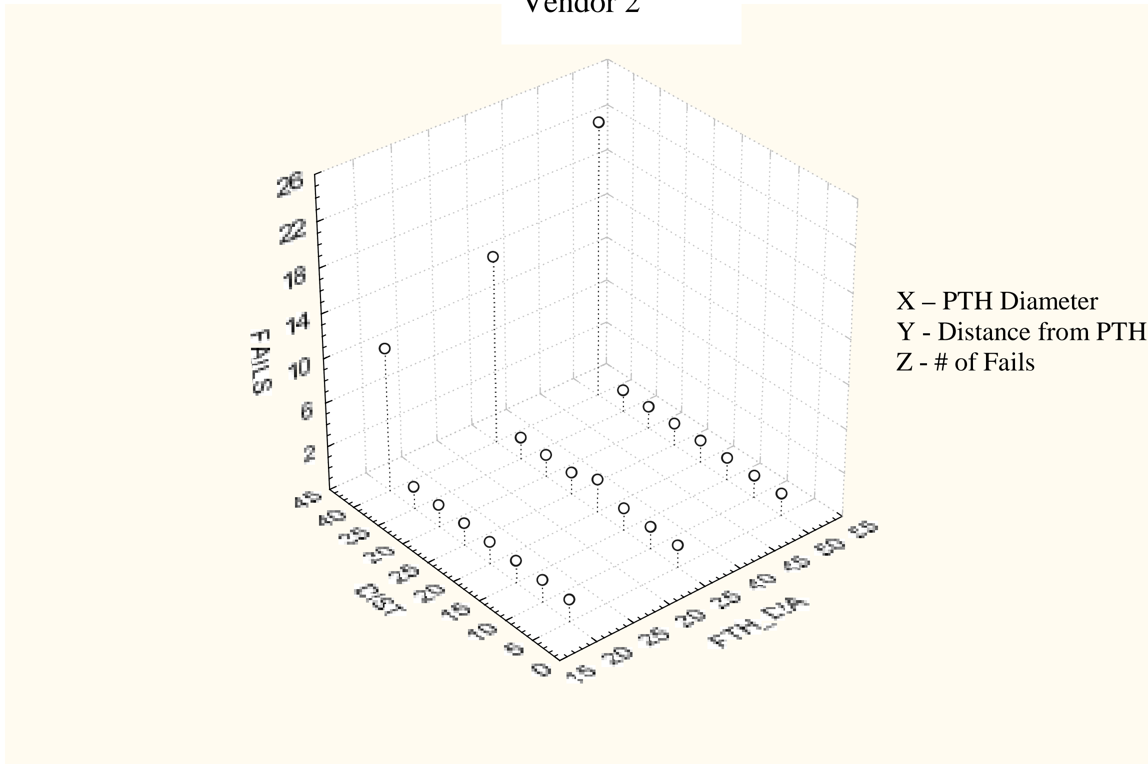
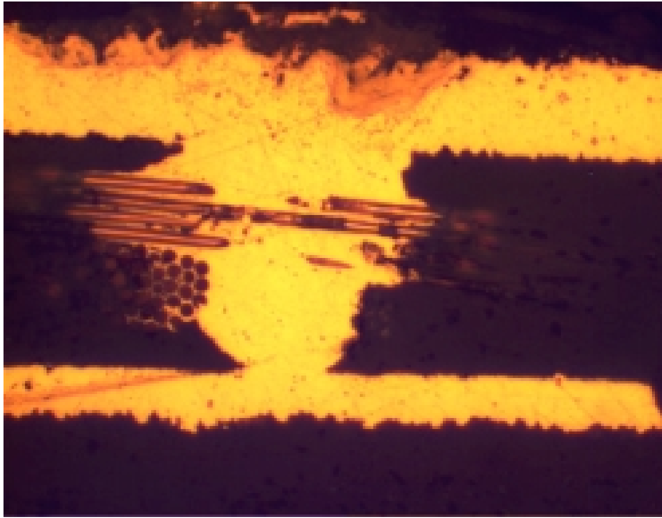
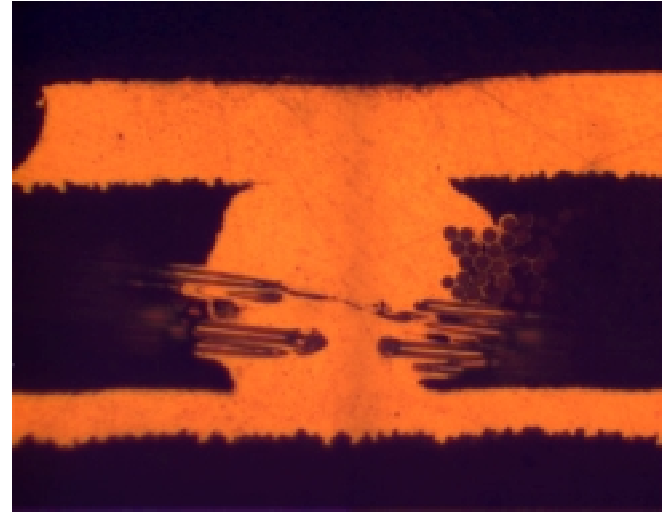


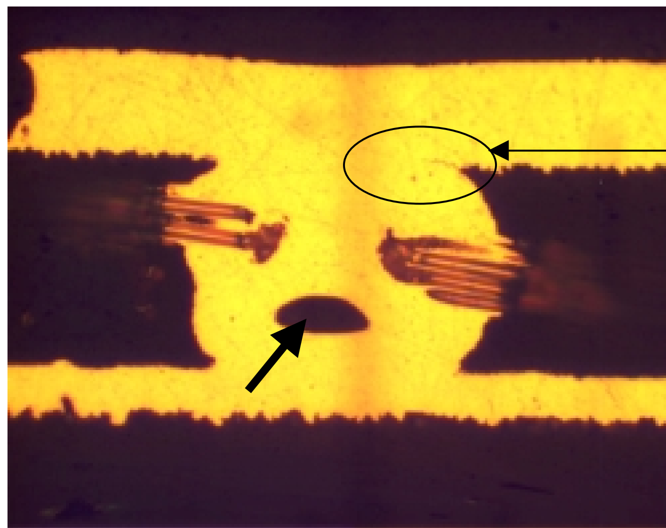
Figure 4. Failure Frequency Plot for the Vendor 2



a. Failed Microvia at a Distance of 40 mils from a 20 mil PTH after 1100 LLTS Cycles



b. Failed Microvia at a Distance of 40 mils from a 50 mil PTH after 2000 LLTS Cycles



c. Cross Section of a Via Showing a Void in the Copper Plating

Figure 5. Cross-Sections of Failed Microvias after Different Stages of LLTS Testing (Vendor 2)

Vendor 1

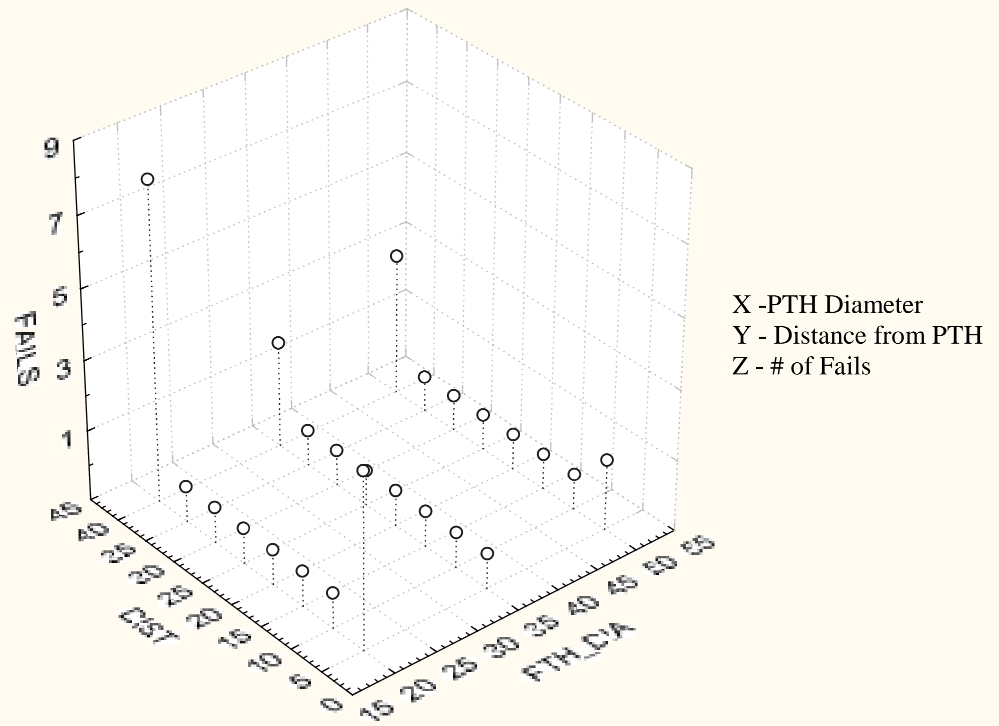
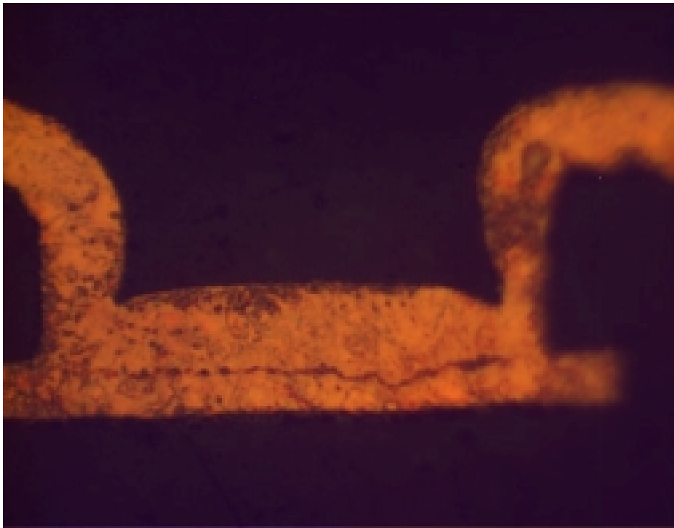


Figure 6. Failure Frequency Plot for Vendor 1



a. Failed Microvia after 1100 LLTS Cycles

b. Functional Via after 2000 LLTS Cycles

Figure 7. Cross-Sections of the Microvias after Different Stages of LLTS Testing

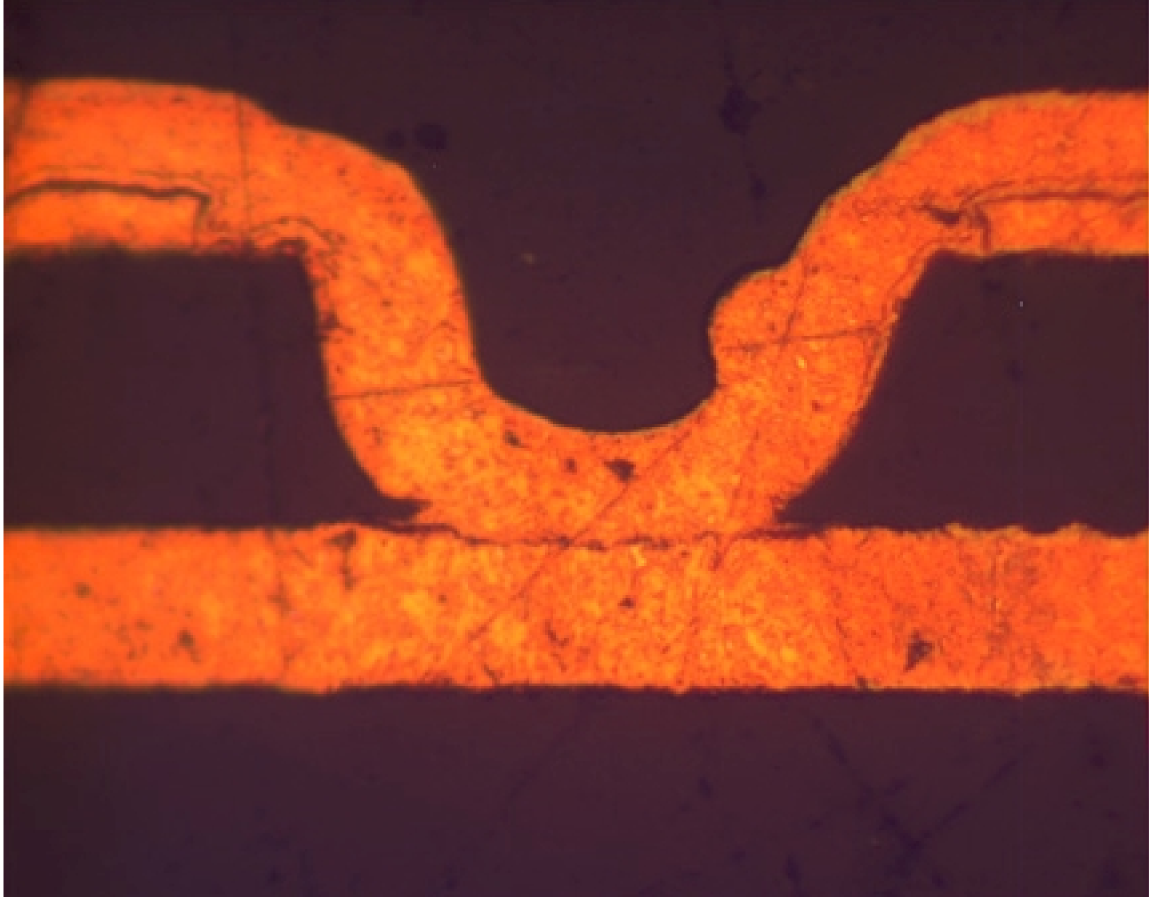
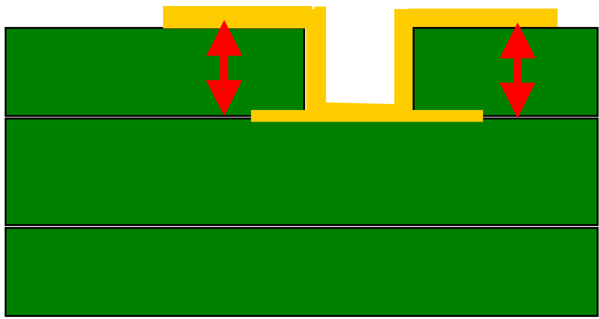


Figure 8. Cross Section of a Failed Via after 1100 LLTS Cycles



Expansions Experienced by the Top Dielectric Layer Cause the Failure at Via and Stop Pad

Vias at the Distance of 40 mils from PTH

e Distance of 5 mils from PTH

Local Z Axis Constraints on the Outer Dielectric Layer around PTH

Figure 9. Failure Mechanism for the Higher Frequency of the Failures of Vias at the Distance of 40 mils from the PTH

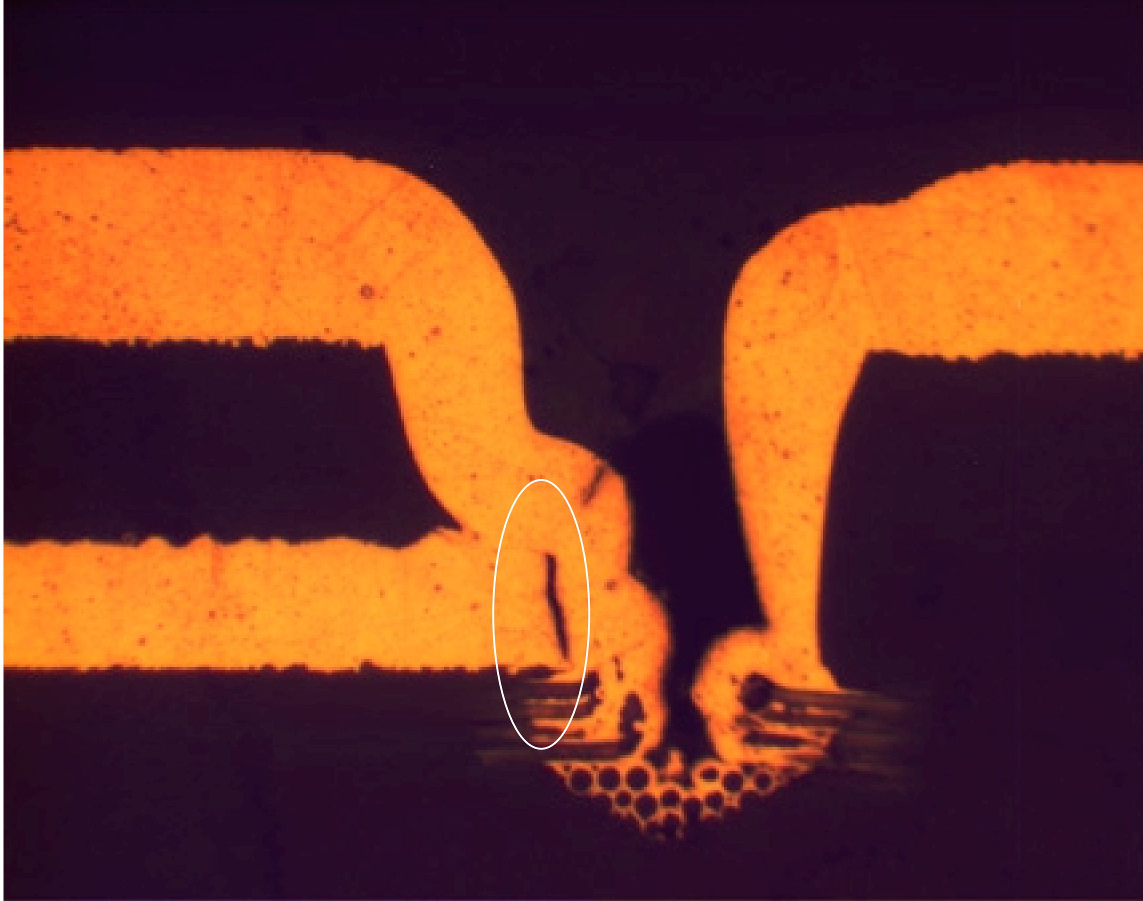


Figure 10. Cross Section of a Via that Failed due to Misregistration to the Stop Pad

Via Hole Formation Technology	**Dielectric Material**	**Failure Mechanism**
YAG Laser (Vendor 3)	Glass Reinforced	I. No Failures for 2000 LLTS Cycles
YAG Laser (Vendor 1)	Non Reinforced	I. Crack at the Via Pad Interface
YAG+CO2 Laser (Vendor 3 & 4)	Glass Reinforced	I. Improper Cleaning of the Glass Fibers II. Crack Through the Via
Photodefined (Vendor 2)	Non Reinforced	I. Crack at the Via Pad Interface

Table 1. Summary of Board Parameters and Failure Mechanism

Pad to Pad Distance (mils)	Effective Center to Center Distance Between a Via and a PTH (mils)		
	50 mil PTH	35 mil PTH	20 mil PTH
5	45	36	27
10	50	41	32
15	55	46	37
20	60	51	42
25	65	56	47
30	70	61	52
35	75	66	57
40	80	71	62

Table 1a. Effective Center to Center Distance Between a Via and a PTH

PTH Size	Distance From PTH	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
50 mils	5 mils										
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils	2		2	6	3					10
PTH Size	Distance From PTH	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
35 mils	5 mils										
	10 mils										
	15 mils										
	20 mils		1								
	25 mils										
	30 mils										
	35 mils										
	40 mils				4	1					10
PTH Size	Distance From PTH	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
20 mils	5 mils										
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils	2		2		3					4

Table 2. Number of Failed Vias in the Samples Provided by Vendor 4 for Testing

PTH Size	Distance from PTH	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
50 mils	5 mils	1									
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils		1								2
PTH Size	**Distance from PTH**	**1100**	**1200**	**1300**	**1400**	**1500**	**1600**	**1700**	**1800**	**1900**	**2000**
35 mils	5 mils										4
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils		1			1					
PTH Size	**Distance from PTH**	**1100**	**1200**	**1300**	**1400**	**1500**	**1600**	**1700**	**1800**	**1900**	**2000**
20 mils	5 mils				2						2
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils		1		1	1					5

Table 3. Number of Failed Vias in the Samples provided by Vendor 1 for Testing

PTH Size	Distance from PTH	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
50 mils	5 mils										
	10 mils										
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils	1				1					
PTH Size	**Distance from PTH**	**1100**	**1200**	**1300**	**1400**	**1500**	**1600**	**1700**	**1800**	**1900**	**2000**
35 mils	5 mils										
	10 mils										
	15 mils					1					
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils										
PTH Size	**Distance from PTH**	**1100**	**1200**	**1300**	**1400**	**1500**	**1600**	**1700**	**1800**	**1900**	**2000**
20 mils	5 mils										
	10 mils				1						1
	15 mils										
	20 mils										
	25 mils										
	30 mils										
	35 mils										
	40 mils										

Table 4. Number of Failed Vias in the Samples from Vendor 2 that were Tested